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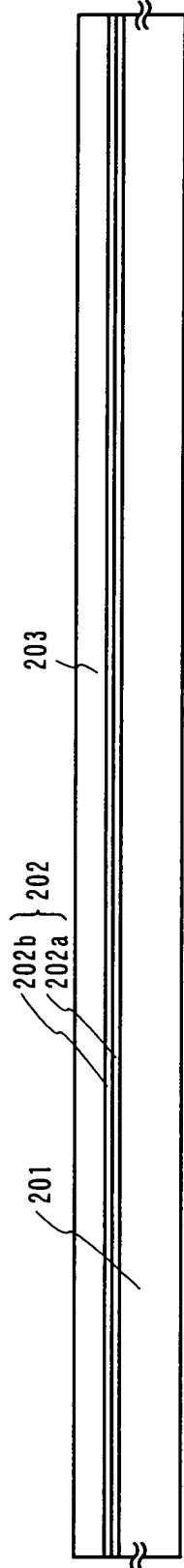


Fig. 2A

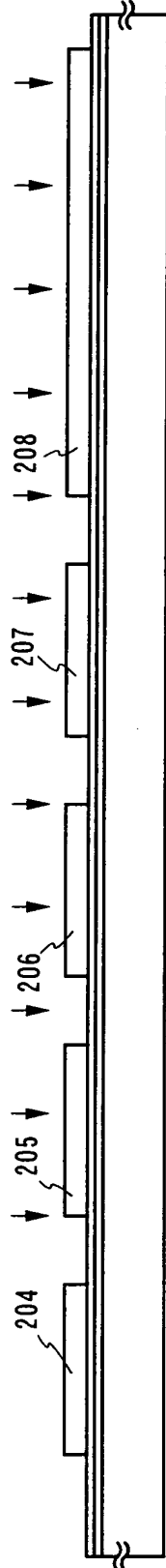


Fig. 2B

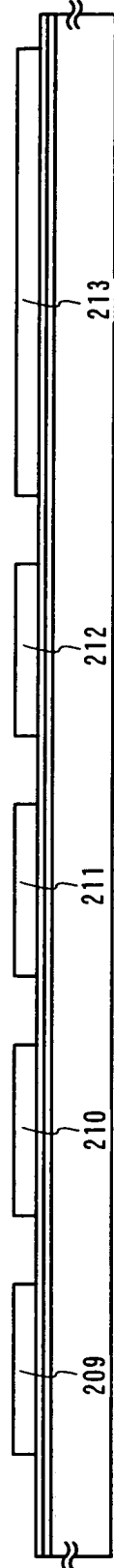


Fig. 2C

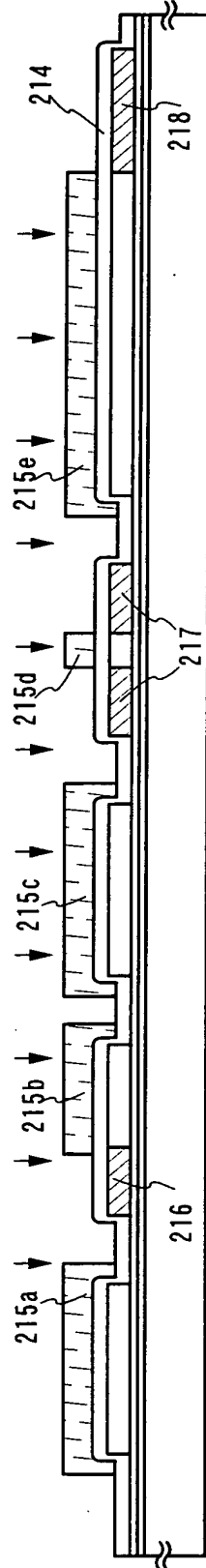


Fig. 2D

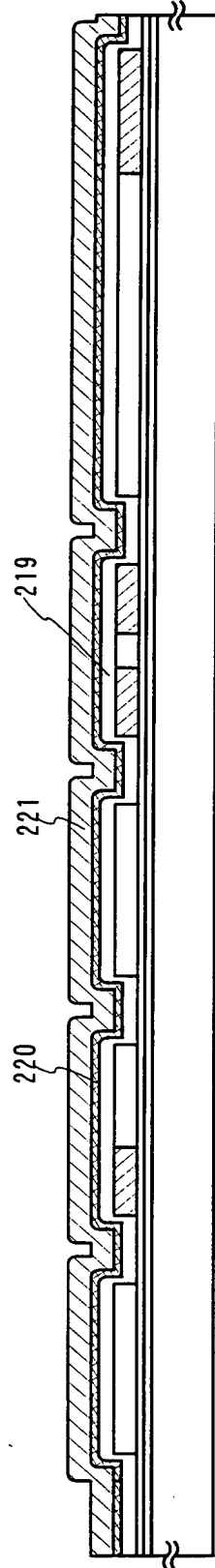


Fig. 2E

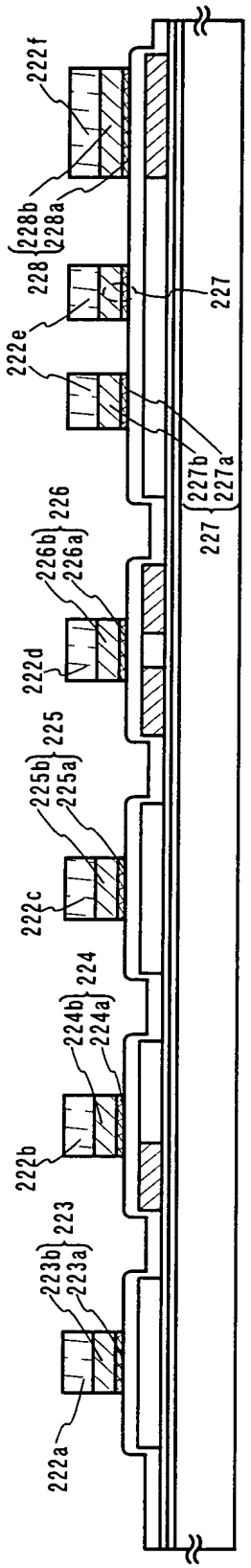


Fig. 3A

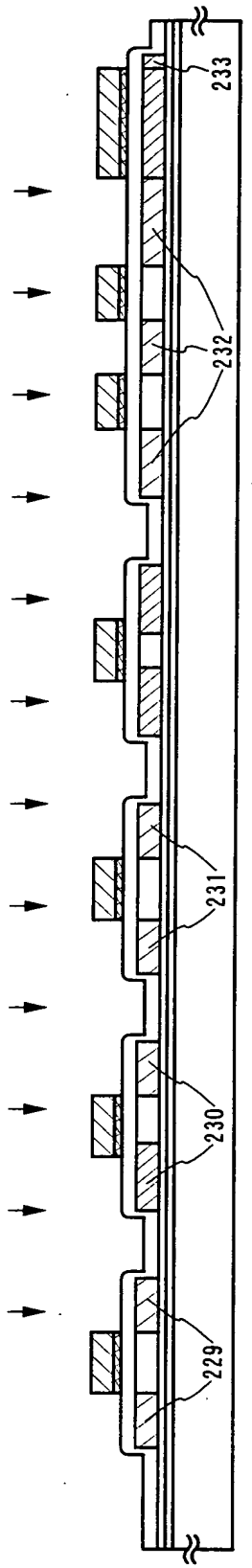


Fig. 3B

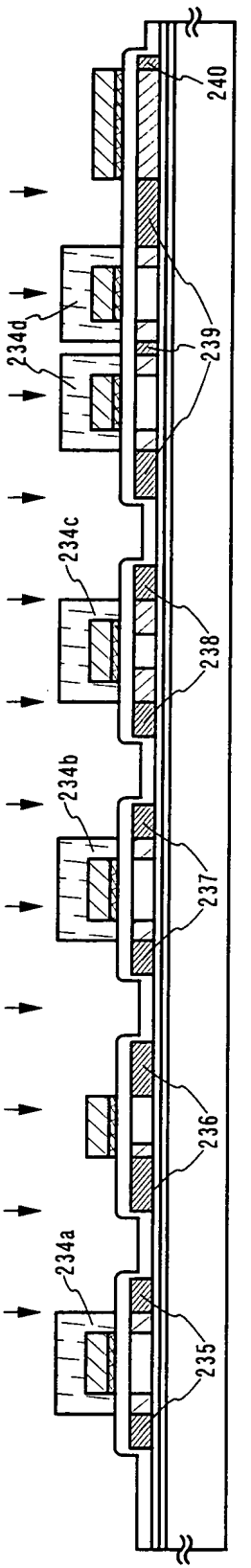


Fig. 3C

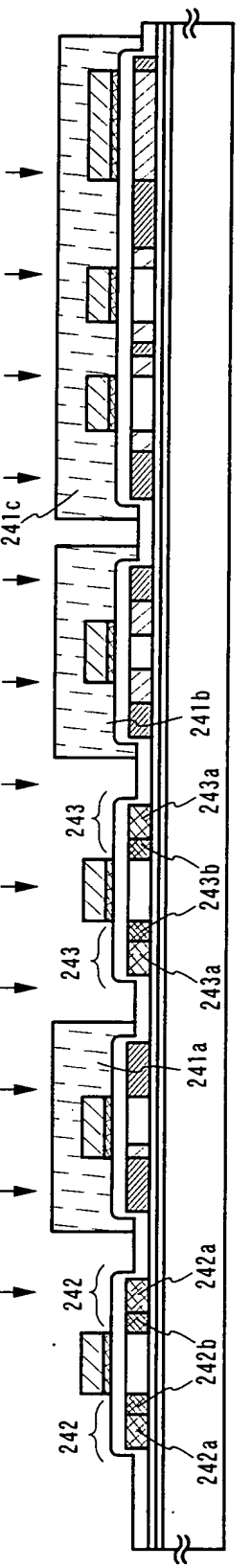


Fig. 3D

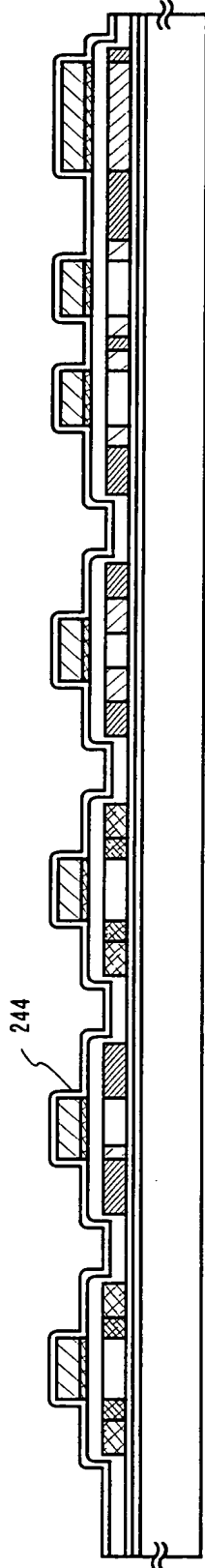


Fig. 4A

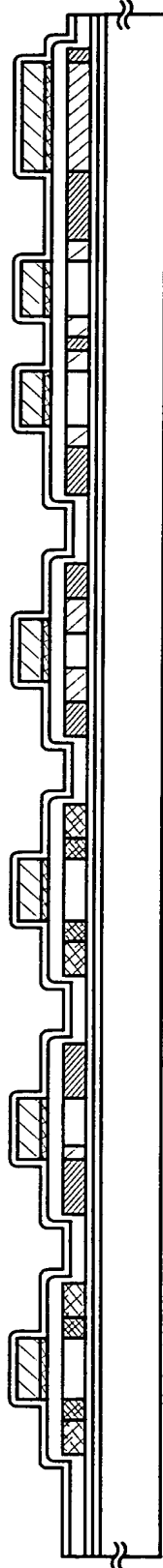


Fig. 4B

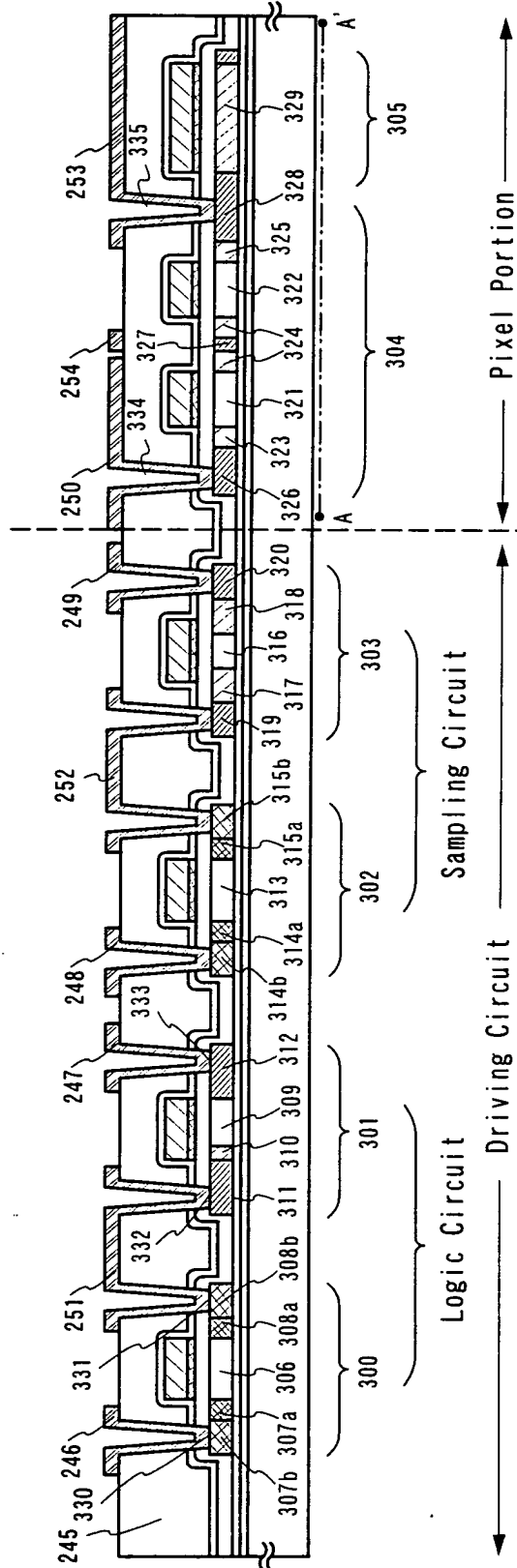


Fig. 4C



Fig. 6A

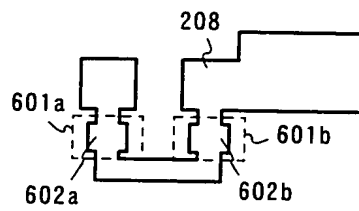


Fig. 6B

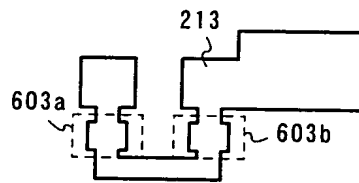


Fig. 6C

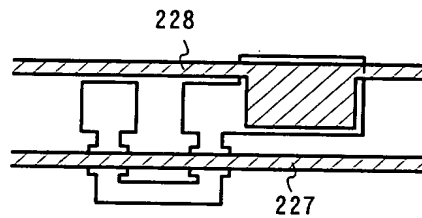
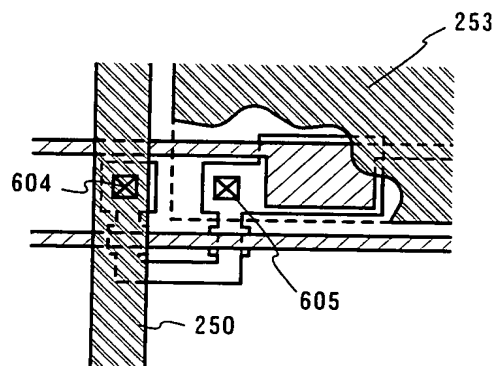


Fig. 6D



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Fig. 7A

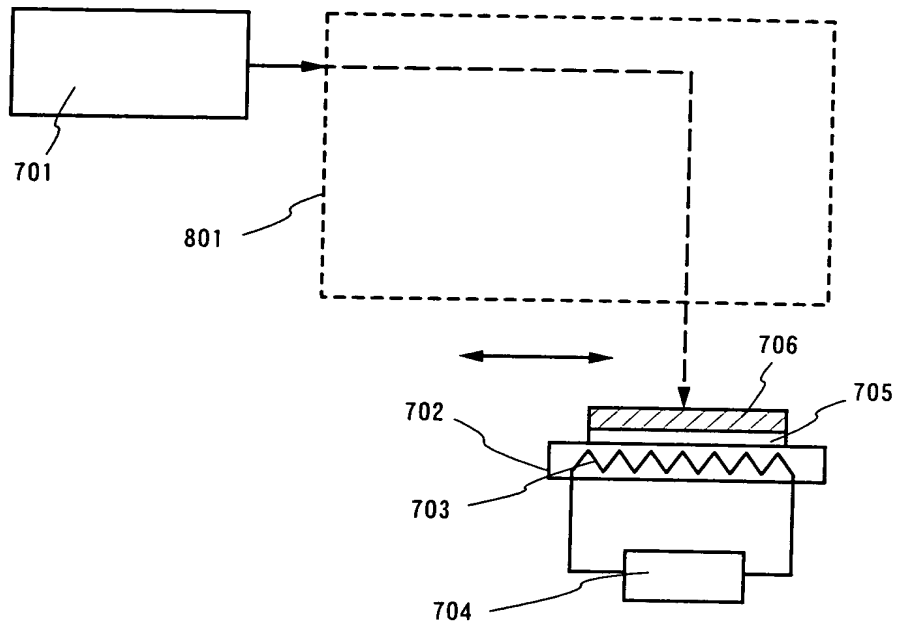
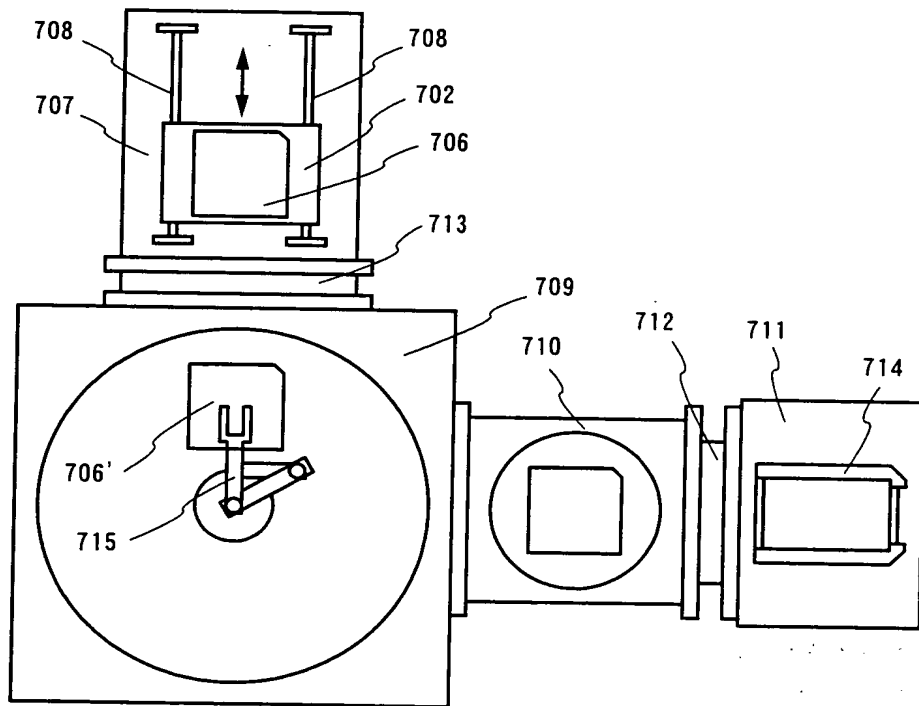
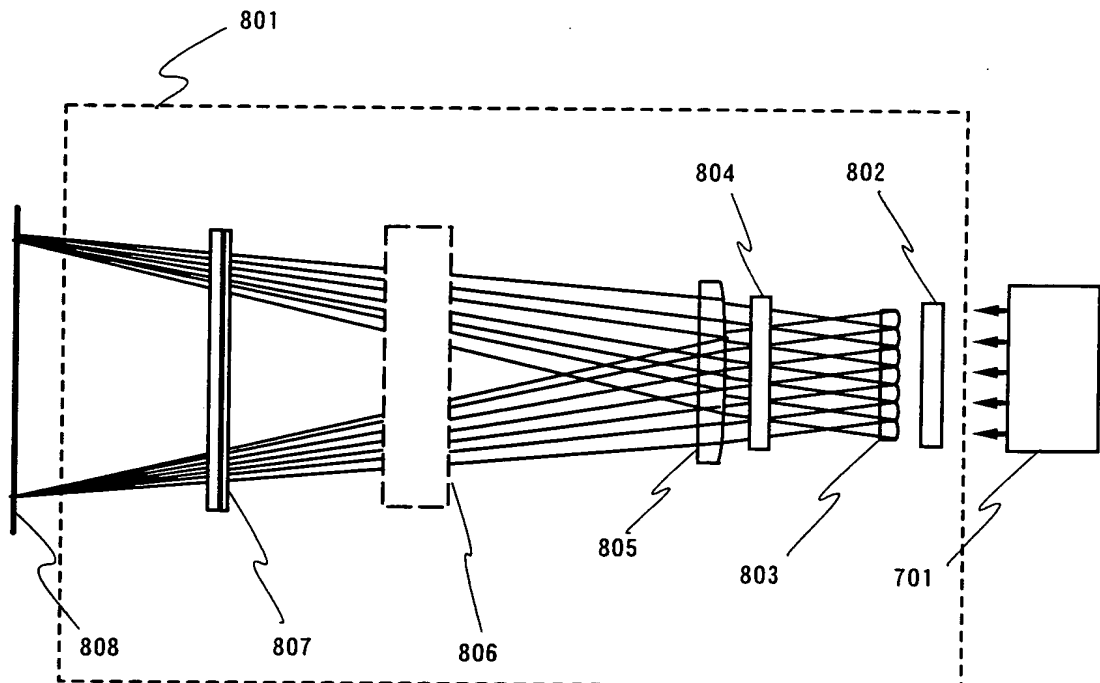
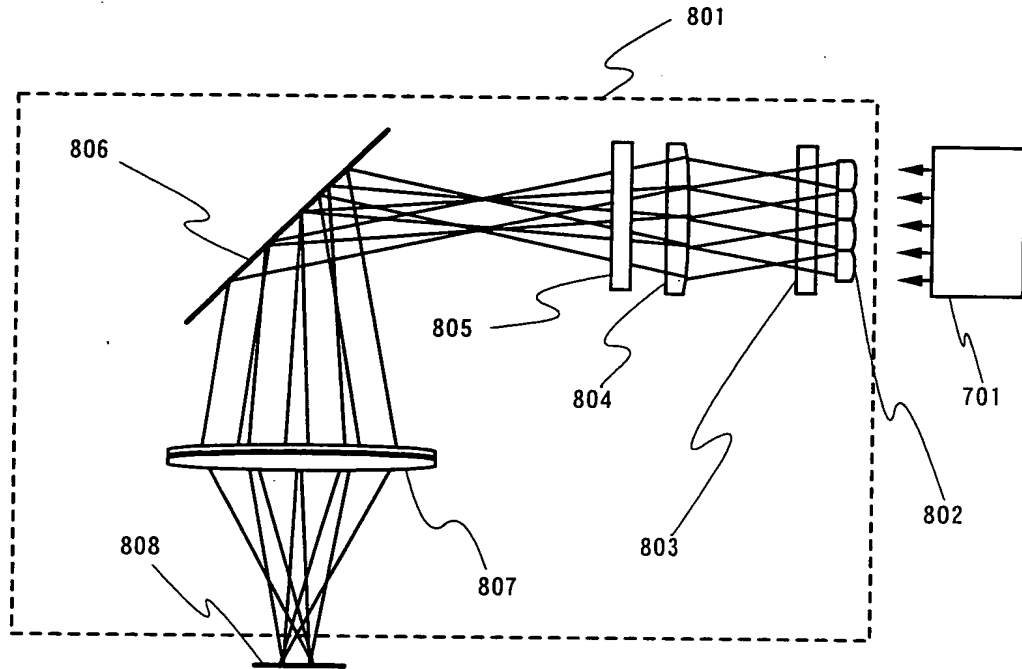


Fig. 7B



12.4.

**Fig. 8B**  
(Top View)



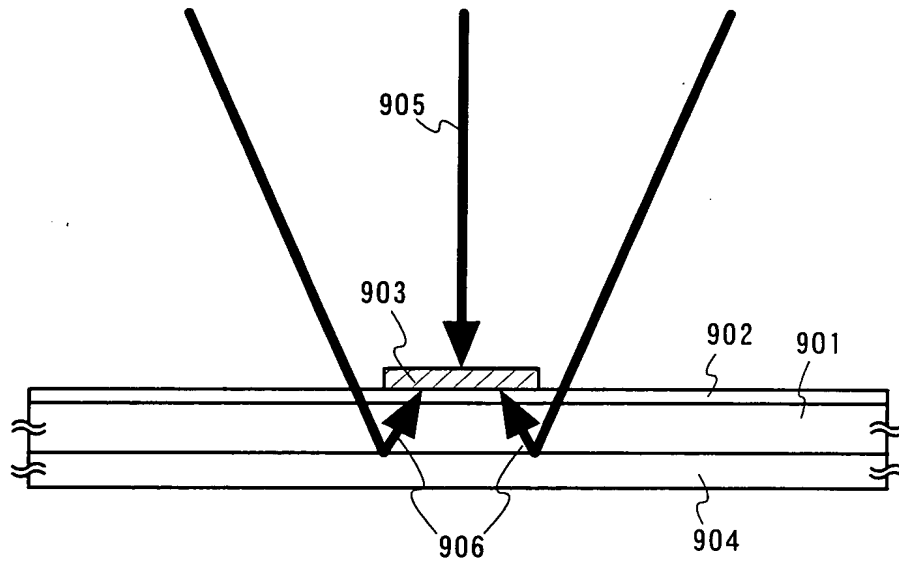


Fig. 9

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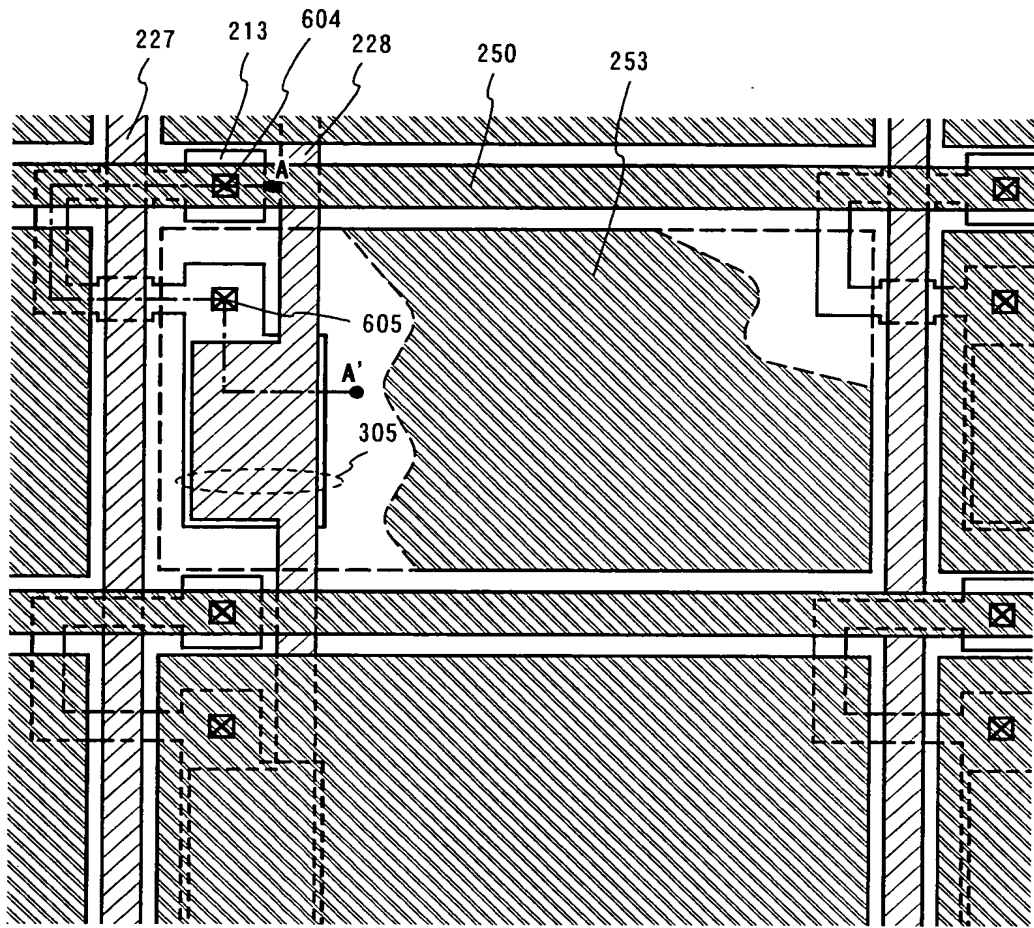


Fig. 10

This cross-sectional view shows a multi-layered semiconductor device. A central core (403) is composed of alternating horizontal layers of different materials, indicated by diagonal hatching and horizontal line patterns. This core is flanked by vertical side walls (404) that also exhibit a layered structure. On the top surface, there is a series of rectangular features (406) separated by recessed channels (409). A thin, uniform layer (405) covers the entire top surface of the device. A circular feature, possibly a contact or a probe, is shown on the right side of the top surface. The device is shown in a perspective view with break lines at the top and bottom.

Fi. 11B

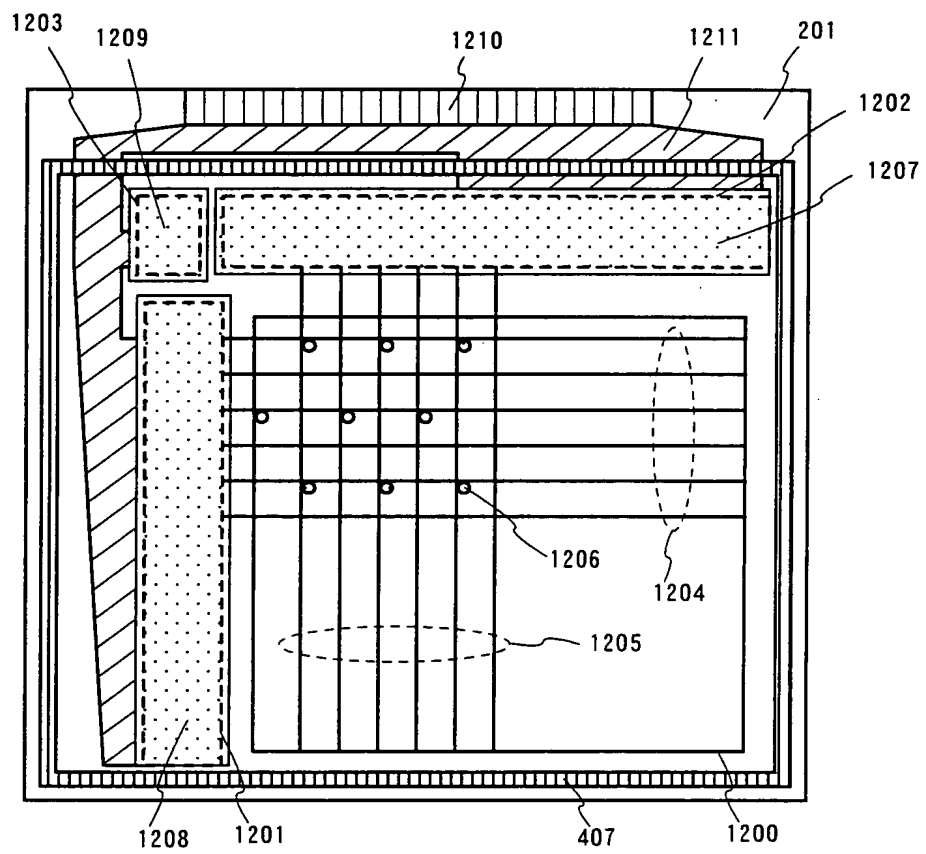


Fig. 12



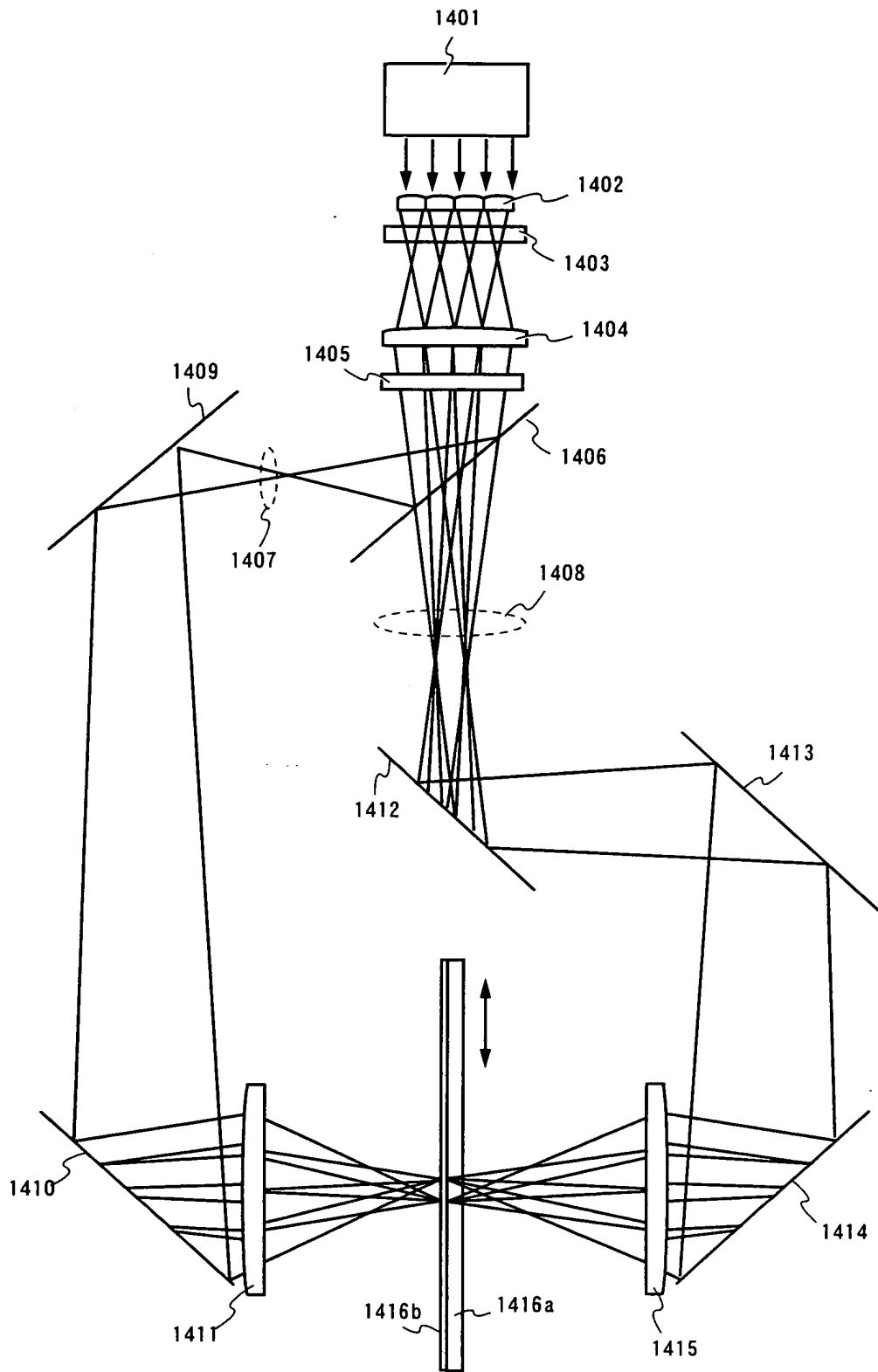


Fig. 14

Fig. 15A

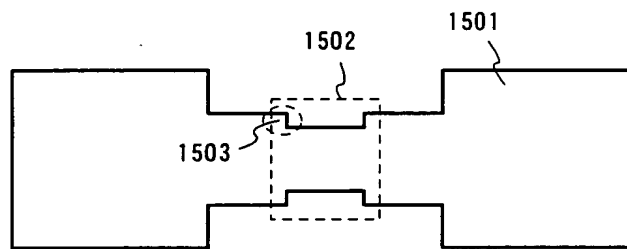


Fig. 15B

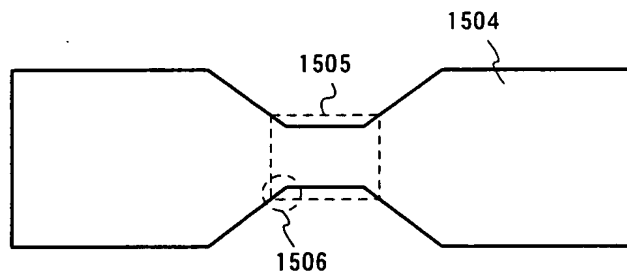
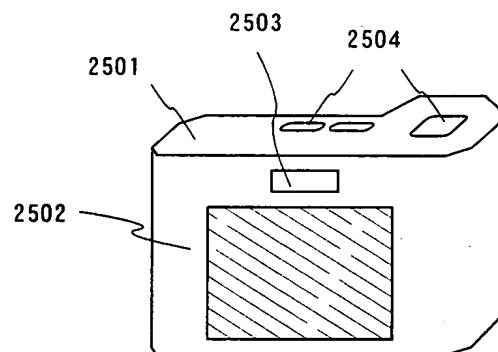
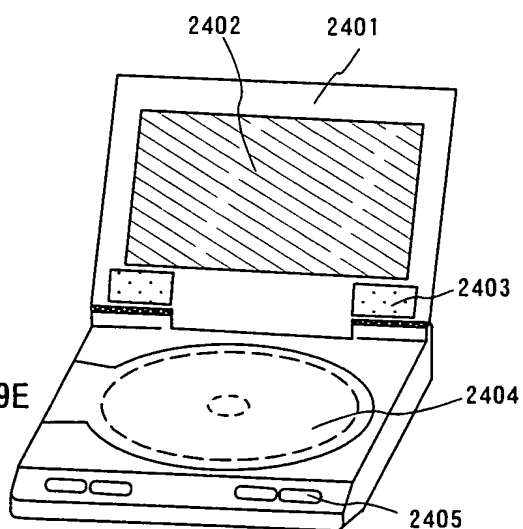
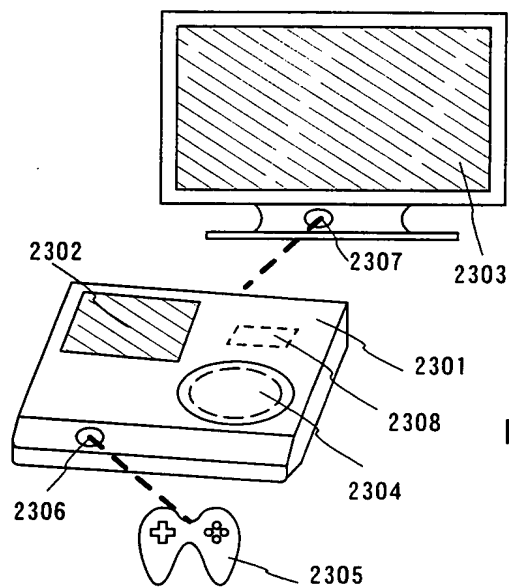
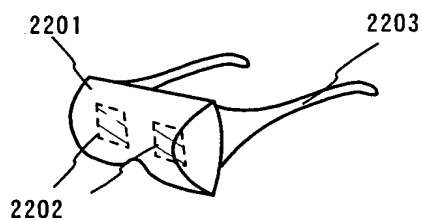
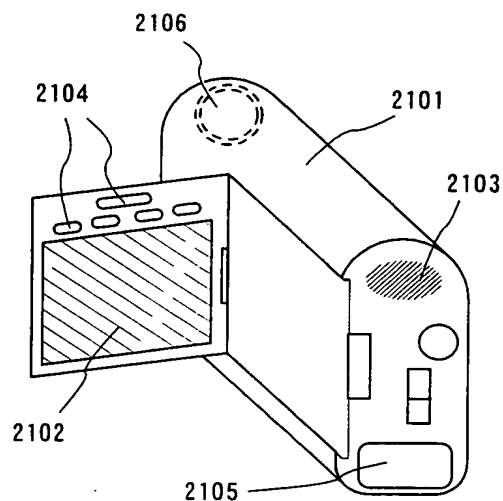
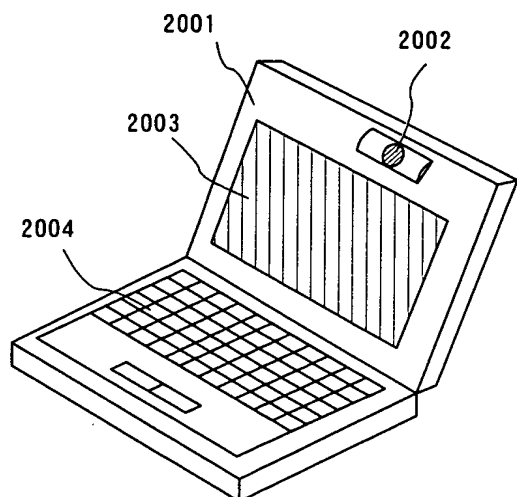






Fig. 18B



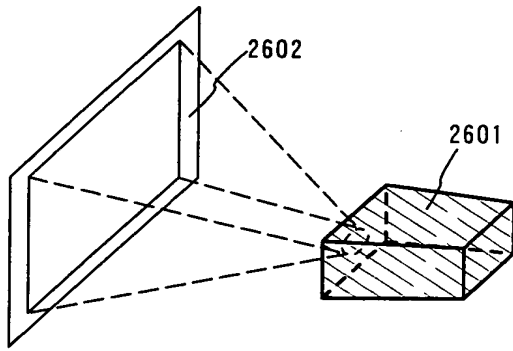


Fig. 20A

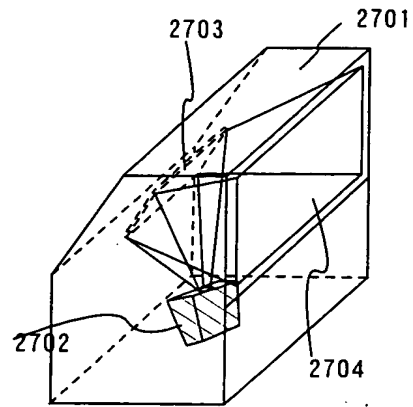


Fig. 20B

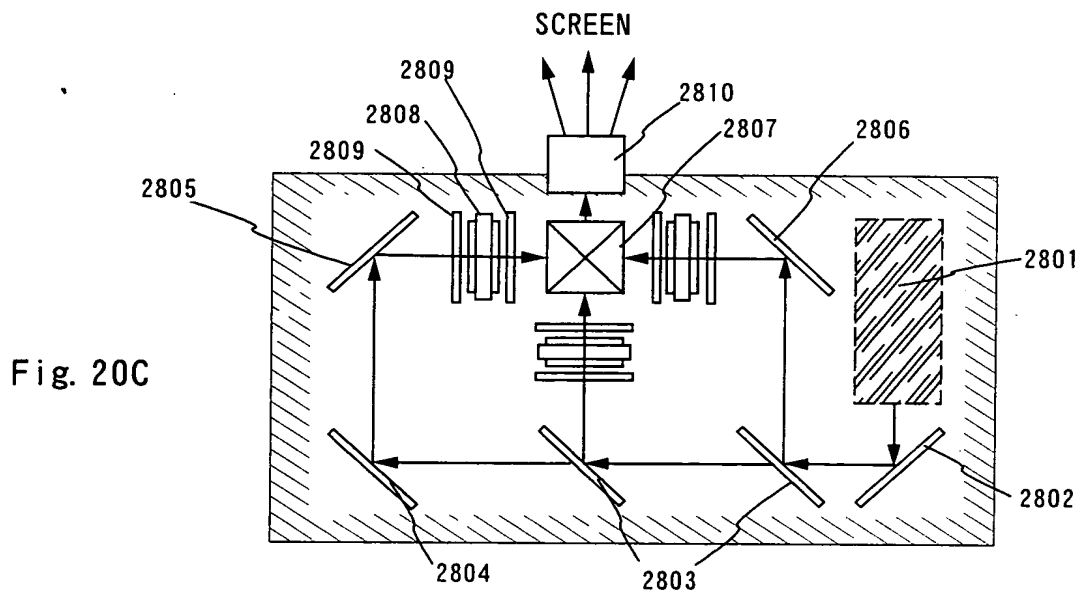


Fig. 20C

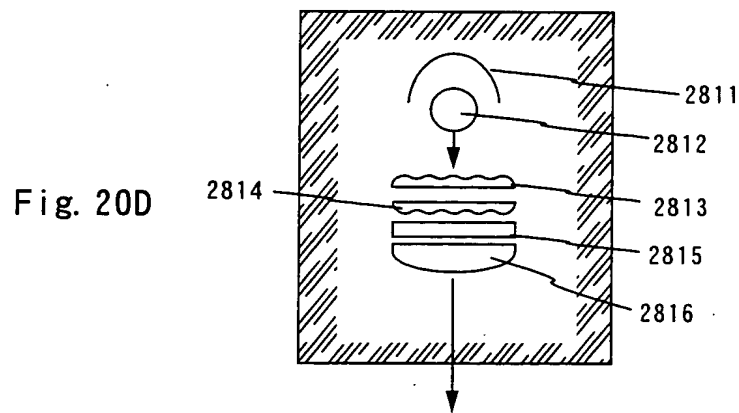


Fig. 20D

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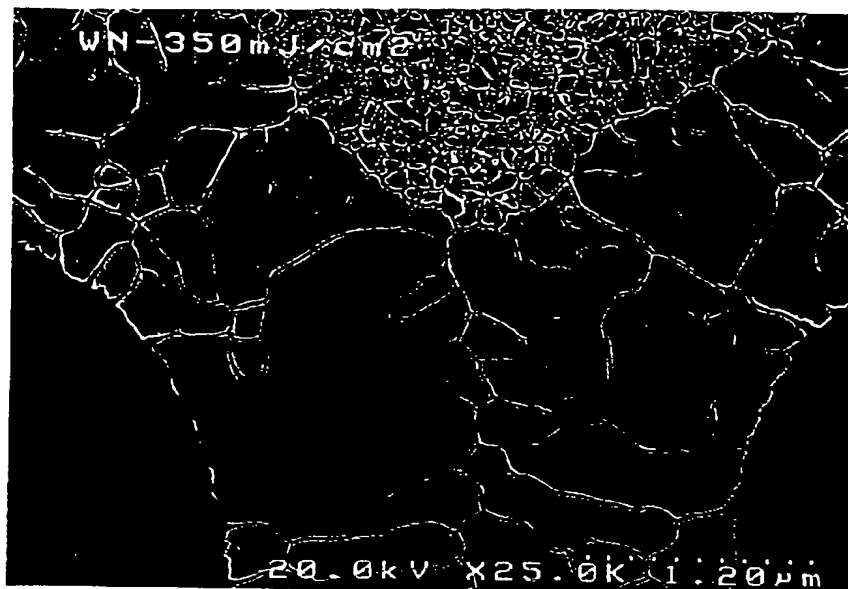


Fig. 21